Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). A [[PLL]] phase locked loop circuit comprising:

a phase comparator for comparing a reference frequency of an external clock signal with a comparison frequency of a comparison clock signal;

a filter for filtering an output signal from the phase comparator;

a [[VCO]] voltage controlled oscillator for generating a clock signal [[of]] having a frequency proportional to a DC signal from the filter;

a prescaler for ~~selectively~~ dividing [[the]] an output clock signal from the voltage ~~control~~ controlled oscillator by using at least two ~~or more~~ division ratios;

a program counter for dividing an output signal from the prescaler [[with]] by a ~~predetermined~~ division ratio[[,]] and outputting the comparison clock signal having the comparison frequency;

a swallow counter for controlling the division ratio of the prescaler; [[and]]

a controller for controlling the prescaler by using output signals from the program counter and the swallow counter; and

a control signal generator for outputting a control signal to control frequency division of the [[VCO]] voltage controlled oscillator by using set points of the prescaler, the swallow counter, and the program counter.

Claim 2 (currently amended). The [[PLL]] phase locked loop circuit according to claim 1, wherein the prescaler is set at ~~large~~ a larger one of the at least two ~~or more~~ division ratios while the swallow counter operates.

Claim 3 (currently amended). The [[PLL]] phase locked loop circuit according to claim [[2]]1, wherein the prescaler is set at ~~small~~ a smaller one of the at least two ~~or more~~ division ratios [[when]] after the swallow counter counts a ~~pulse by~~ number of pulses corresponding to the set point[[.]] of the swallow counter.

Claim 4 (cancelled).

Claim 5 (currently amended). The [[PLL]] phase locked loop circuit according to claim [[4]]1, wherein the ~~decoder~~ control signal generator is configured using [[the]] a bit number of ~~output bits~~ the control signal, the whole counter set point, the swallow counter set point and the program counter set point.

Claim 6 (currently amended). The [[PLL]] phase locked loop circuit according to claim 5, wherein the bit number of the control ~~output~~ signal is determined by determining a voltage profit of the [[VCO]] voltage controlled oscillator when the set point of the prescaler is set,

wherein the whole counter set point of corresponding frequency is determined, and wherein the swallow counter set point and the program counter set point corresponding to the whole counter set point are determined.